

### REMARKS

Claims 8-13, 19, 21, and 28-35 are presented for further examination. Claims 8, 19, 28, and 32 have been amended.

In the final Office Action mailed February 5, 2009, the Examiner rejected claims 8-13 under 35 U.S.C. § 103(a) as obvious over previously-cited Sidner et al. in view of Mirza et al. Claims 28, 29, 32, and 33 were rejected under 35 U.S.C. § 102(b) as anticipated by Mirza et al. Claims 30, 31, 34, and 35 were rejected as obvious over Mirza et al. in view of previously-cited Beyer et al. Claims 19 and 31 were rejected as obvious over Mirza et al. in view of Sidner et al.

Applicants respectfully disagree with the bases for the rejections and request reconsideration and further examination of the claims.

### Withdrawal of Finality of Office Action

Upon review of the Office Action mailed February 5, 2009, applicants noted that claim 21 was not addressed by the Examiner. During a telephone conference with the Examiner on March 25, 2009, to discuss this issue, the undersigned attorney was told by the Examiner to file a response and note that the finality was improper because the basis for the rejection of claim 21 was not set forth in the action. Applicants respectfully request withdrawal of the finality of the Office Action mailed February 5, 2009, because the basis for the rejection of claim 21 was not set forth in the action.

### Claim Rejections

Independent claims 8, 19, 28, and 32 have been amended to clearly recite the use of an epitaxial layer grown on the monocrystalline silicon substrate to close the trenches and form a membrane over each of the resulting cavities formed in the substrate. Support for this amendment can be found throughout the specification. For example, at page 5, lines 3-9, 21-22, and 29, all clearly describe the use of an epitaxial growth in which “monocrystalline silicon is grown horizontally, inside the first trenches 15, thus closing the latter, and vertically, from the surface 11 (which can no longer be seen in Figure 12).”

The use of an epitaxial grown layer to enclose the trenches and form the membrane overcomes the disadvantages of using a bonded layer as described in the Background of the Invention portion of the pending application. The use of bonded materials is costly, has a high criticality and low productivity, and is not fully compatible with the usual technological steps of microelectronics processing (see page 1, lines 19-21).

In contrast, Mizra et al. describe a cavity 13 that is formed in a silicon substrate 11 is covered with a diaphragm formed by a second silicon substrate 17 that is “bonded” over the top surface 12 of the first substrate. In view of the foregoing, applicants respectfully submit that claims 28, 29, 32, and 33 are not anticipated by Mirza et al.

Likewise, claims 30, 31, 34, and 35 are allowable over the combination of Mirza et al. and Beyer et al. for the reasons discussed above with respect to Mirza et al. and further because Beyer et al. does not teach or suggest an epitaxial growth to form a membrane over a cavity. Rather, Beyer et al. specifically teaches that a void-free isolation structure is essential to accomplishing the purposes of Beyer et al., which is to create an isolation structure. Thus, the purposes of Mirza et al. and Beyer et al. are at odds with each other and one of ordinary skill would find no teaching or suggestion for combining these two references in the manner suggested by the Examiner.

Turning next to claims 19 and 31, these two claims are rejected as obvious over Mirza et al. in view of Sidner et al. As previously discussed, Mirza et al. is directed to the use of two substrates that are bonded together. Mirza et al.’s goal is to form a sensor “that does not require a bonding process in an oxygen rich or vacuum ambient” (see Abstract). Rather, Mirza et al. specifically teaches that “As part of the bonding operation, first substrate 11 and second substrate 17 are placed in contact with each other under an ambient condition. For instance, the bonding can take place at atmospheric pressure in a clean room ambient.” (See Mirza et al., column 3, lines 5-8). Only after the two substrates are bonded is the structure then placed into an oxidizing ambient to form an oxide layer to close the cavity, thus requiring an additional step. In contrast, the present claimed process utilizes the epitaxial growth to also seal the cavity, thus eliminating an additional step taught by Mirza et al.

The combination of Sidner et al. with Mirza et al. as suggested by the Examiner is directly contrary to the process taught by Mirza et al. The Examiner relies upon Sidner et al. to teach the membrane having a thickness in the range of 1-10 microns. However, in Mirza et al., after the cavity 13 is sealed, “piezoresistors 21 are formed in the second substrate 17” (see column 4, lines 7-8). As shown in Figure 1, these resistors 21 clearly overlap with the cavity. There is insufficient thickness to form such resistors if the structure of Mirza et al. were in the range of 1-10 microns. In view of the foregoing, applicants respectfully submit that claims 19 and 31 are clearly allowable over the combination of Mirza et al. and Sidner et al.

Turning next to claims 8-13, claim 8 now recites an epitaxial layer of semiconductor material grown horizontally and vertically on the substrate to cover the open top of the at least one trench and formed in the at least one trench to fill the at least one trench and to encase the cavity in the substrate. Applicants note that in Sidner et al., the closing of the neck portion 34 of the cavity is done with a process that utilizes lateral growth rather than vertical growth so as not to fill up the cavity (see column 5, lines 36-40: “The deposition conditions are chosen to favor lateral growth rather than vertical growth so that the neck opening 34 can be filled without materially affecting the remainder of cavity 16.”).

Hence, there is no need for a coating on the walls of Sidner et al.’s cavity to inhibit vertical epitaxial growth. The Examiner’s suggestion of modifying Sidner et al. with the coating of Mirza et al. does not achieve the claimed horizontal and vertical growth of epitaxial layer as recited in claim 8 because Mirza et al. fails to teach this feature as well as how to apply this feature to the structure of Sidner et al. without defeating the purpose of Sidner et al.

In view of the foregoing, applicants respectfully submit that all of the claims in this application are now in condition for allowance. In the event the Examiner disagrees or finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact the undersigned by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

Application No. 10/667,113  
Reply to Office Action dated February 5, 2009

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,  
SEED Intellectual Property Law Group PLLC

/E. Russell Tarleton/  
E. Russell Tarleton  
Registration No. 31,800

ERT:alb

701 Fifth Avenue, Suite 5400  
Seattle, Washington 98104  
Phone: (206) 622-4900  
Fax: (206) 682-6031

854063.552D1 / 1382458\_1.DOC